1   IF FSK RECEIVER

CROSS-REFERENCE TO RELATED APPLICATIONS

        This patent application claims the benefit of the filing
5   date of United States Provisional Patent Application Serial No.
60/253,268, filed November 27, 2000 and entitled "IF FSK
DEMODULATOR"; the entire contents of which are hereby expressly
incorporated by reference.

10   FIELD OF THE INVENTION

        The present invention relates to communication systems.
More specifically, the invention relates to signal demodulation.

BACKGROUND OF THE INVENTION

15   Some radio transmission standards such as, the Bluetooth
standard, specify a 2.4 GHz frequency-hopped, spread-spectrum
system using a Gaussian-FSK (GFSK) modulation scheme with a data
rate of 1 Mb/sec. The frequency offsets are ±160 kHz,
corresponding to a nominal modulation index of 0.32 and the data
20   bandwidth is about 1 MHz. Consequently, an exemplary Bluetooth
receiver has a 2 MHz intermediate frequency (IF), causing the
image signal to be within the 80 MHz ISM band. The image reject
requirement is therefore relaxed, and may be achieved by an on-
chip complex-domain bandpass filter (BPF). Once the desired
25   channel is selected, a limiter amplifies it to a well-defined
level, and the received signal strength is indicated.

        A commonly used type of pulse-code modulation is FSK, in
which the carrier frequency changes abruptly by an amount Δf as
the modulating signal changes from the zero level to the one
30   level, or vice versa. A FSK demodulation typically uses a
differentiator followed by I and Q multipliers. However, if
implemented at base-band, the desired signal at 2 MHz is down-
converted to zero IF. This approach needs to use four additional
mixers for single side-band, quadrature downconversion, and a 2
35   MHz clock generator. This increases the receiver power

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1   dissipation, and leads to a larger silicon area. Additionally,
     the base-band demodulator is more susceptible to DC offset and
     low frequency noise and interference.

         Typically, an analog differentiator followed by an envelope
5   detector can be used to detect an FM modulated signal. This is
     simple and low-power, however, its performance is limited due to
     the inaccuracy of the components once realized in an IC. In
     contrast, an FSK demodulator may be implemented digitally, which
     is more robust, yet it consumes more power, and is more complex.

10   Moreover, a direct-conversion receiver also has few
     disadvantages. For example, since the GFSK spectrum has energy
     at zero IF, DC offset and 1/f noise may degrade the receiver
     performance. Also, a limiter at base-band is generally not
     suitable for a GFSK signal down-converted to zero IF, since the
15   harmonics of the limited signal fall inside the desired band,
     degrading the receiver BER. This problem may be evaded if the
     limiter is substituted by an automatic gain controller (AGC).
     However, an AGC is complicated and consumes more power.

         Therefore, there is a need for a radio transceiver having
20   the characteristics of low size, cost and power. Furthermore,
     there is a need for a receiver including an analog demodulator
     and a differentiator that operate at an IF frequency rather than
     a baseband frequency.

25   SUMMARY OF THE INVENTION
         In one embodiment, the present invention describes a low-
     power, and high performance receiver including an IF demodulator
     for high data rate, frequency modulated systems, such as
     Bluetooth. The IF demodulator is implemented in analog domain
30   for simplicity and lower power consumption and operates at an IF
     frequency.

         In one aspect, an IF demodulator comprising: a first IF
     differentiator for differentiating an I signal; a second IF
     differentiator for differentiating a Q signal; a cross-coupled
35   multiplier for multiplying the differentiated I signal with the

1   I signal and multiplying the differentiated Q signal with the Q
     signal to extract frequency information from the I signal and the
     Q signal; and a slicer for converting the frequency information
     to digital data is disclosed in the present invention.

5   In another aspect, a method for demodulating an IF FSK
     signal comprising the steps of: receiving an IF I signal input
     and an IF Q signal input; differentiating the I signal at the
     frequency of the I signal by a first IF differentiator;
     differentiating the Q signal at the frequency of the Q signal by

10   a second IF differentiator; multiplying the differentiated I
     signal with the I signal and multiplying the differentiated Q
     signal with the Q signal for extracting frequency information
     from the I signal and the Q signal; and converting the frequency
     information to digital data is described in the present

15   invention.

     BRIEF DESCRIPTION OF THE DRAWINGS
          The objects, advantages and features of this invention will
     become more apparent from a consideration of the following

20   detailed description and the drawings, in which:
          FIG. 1 is an exemplary low-IF receiver architecture,
     according to one embodiment of the present invention;
          FIG. 2 is an exemplary block diagram an IF demodulator,
     according to one embodiment of the present invention;

25   FIG. 3 is an exemplary block diagram of an IF
     differentiator, according to one embodiment of the present
     invention;
          FIG. 4 is an exemplary block diagram of an slicer, according
     to one embodiment of the present invention;

30   FIG. 5 is an exemplary simplified circuit diagram of an IF
     differentiator, according to one embodiment of the present
     invention;
          FIG. 6 is an exemplary simplified circuit diagram of a
     multiplier, according to one embodiment of the present invention;

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1   FIG. 7 is an exemplary simplified circuit diagram of an offset tracker, according to one embodiment of the present invention; and

    FIG. 8 is an exemplary simplified circuit diagram of a
5   peak/valley detector, according to one embodiment of the present invention.

DETAILED DESCRIPTION

    To lower the size, cost and power of portable devices with
10 wireless connectivity, all the components are integrated into one single chip. Full integration of a radio transceiver system can reduce cost and power consumption, which can be accomplished by moving the bulky and expensive external image reject, channel select filters and baluns onto a single RF chip and eliminating
15 the number of off-chip passive elements such as capacitors, inductors, and resistors by moving them onto the chip, and integrating all the components including RF, analog, baseband and digital signal processing (DSP) onto the chip.

    The present invention discloses a receiver including an FSK
20 demodulator for use in various applications including Bluetooth. FIG. 1 shows an exemplary low-IF receiver architecture in accordance with an embodiment of the present invention. Low noise amplifier (LNA) 10 amplifies the input signal at 2.4 GHz. Down converters 12 and 14 convert the amplified input signal to
25 a lower frequency signal, for example, a 2 MHz signal by mixing the input signal with respective lower frequency signals LOI and LOQ that are generated locally. A channel selector filter 16 selects a desired channel of frequency. e.g., a 2MHz channel. The channel selector filter is essentially a bandpass filter
30 (BPF) that passes through the selected frequency and rejects the other frequencies.

    Amplifiers 18 and 19 further amplify the I and Q signals respectively. In one implementation, limiters which are a special form of amplifiers are used because they are simpler, low
35 power, and easier to implement. Demodulator 11 exploits the

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1   amplified 2 MHz signal to detect the amplitude of the
    differentiated signal. Since the input signal to the demodulator
    11 is at 2 MHz, the demodulator is designed in such a unique way
    to work at 2 MHz, without having to convert the 2 MHz signal to
5   the baseband signal. An RC calibration 13 circuit monitors
    process variation and mismatch variations and tunes the receiver
    to avoid spurious signals. In one embodiment, the RC calibration
    13 calibrates all the active resistors and capacitors to some
    reference frequency that has a well defined behavior. Self-
10 calibration may be used in the receiver for optimal performance
    and programmed through software.

        FIG. 2 is an exemplary implementation of the demodulator 11
    in FIG. 1. BPF 21 is used to shape the limited input signal
    waveform to a sinusoidal shaped waveform. This BPF rejects the
15 harmonics of the desired channel. Moreover, it attenuates the
    remaining adjacent interference due to the incomplete channel
    selection at the BPF. Differentiators 22 and 23 take the I and
    Q signal and differentiate them to take the frequency information
    (φ(t)) out of the sinusoidal input signals I and Q. However,
20 this frequency information may include some undesired signals and
    noise. The cross-couple multipliers 24 and 25 multiply I and Q
    signals with differentiated Q and I respectively and subtractor
    26 subtracts the multiplied signals so that the sin and cos
    cancel out each other to produce a non-sinusoidal signal A φ(t)
25 plus spurs at the output of the subtractor 26.

        As quadrature signals are available at the demodulator 11
    input, the differentiators 22 and 23 shift their center frequency
    to some desired IF, e.g., 2 MHz. As illustrated in FIG. 3, a
    resistor (R1) connected to the Q (and I) input (jv is the input
30 signal from Q channel) , translates the base-band frequency
    response to an IF set by 1/R1C. The frequency response of the
    IF differentiator is expressed in the following equation:

$$\frac{V_o}{V_i}(jw) = -jRC\left(w - \frac{1}{R_1 C}\right) \qquad (1)$$

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1   Thus, the center frequency of the IF differentiator moves
to 1/R1C. This center frequency may be adjusted by selecting
appropriate values for R1 and C to any IF frequency. In one
implementation the values for R1 and C are selected to obtain an
5   IF frequency of 2 MHz.

       Referring back to FIG. 2, a lowpass filter (LPF) 27 cleans
the demodulated spectrum whose bandwidth is about ± 550 kHz to
get ride of the spurs. The LPF 27 is sharp enough to reject the
undesired signals produced due to the non-ideal mixing action in
10   the multipliers or mismatches, yet wide enough not to filter the
desired signal, or cause settling issues. Following the LPF 27,
a slicer 28 is used to convert the analog detected output to
digital bits.

       FIG. 4 is an exemplary block diagram for the slicer 28 of
15   FIG. 2. As shown in FIG. 4, the slicer includes a peak detector
41, a valley detector 42, an offset tracking circuit 43 at the
output of the peak and valley detector, and a comparator 44 at
the output of the offset tracking. The offset tracking circuit
43 adjusts the DC level of the analog eye by taking the average
20   of the peak and valley detector outputs. Digital eye is produced
by comparing this DC offset to the analog eye.

       A $\varphi(t)$, the analog signal at the input of the slicer 28 in
FIG. 2, is applied to the inputs of the peak detector 41 and the
valley detector 42 in FIG. 4. The peak detector 41 detects the
25   peack of the analog input signal V_P and the valley detector 42
detect the valleys (minimums) of the analog input signal V_V. The
offset tracking circuit 43 takes the average of V_P and V_V ((V_P +
V_V)/2) to produce a DC average of the peak and valley. This DC
average signal is compared with the original analog signal by
30   comparator 44 to produce the desired digital output. At the
output of comparator, a high signal is produced if the analog
input signal is higher than its DC average value, and a low
signal is produced if the analog input signal is lower than its
DC average value. The Slow/Fast signal depicted in FIG. 4

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1   indicates wether the slicer must go to fast attach mode or slow
     decay mode described below.

          Any frequency error caused by the crystal inaccuracy would
     result in a DC component at demodulator 11 analog output.
5   However, since the slicer detects the DC level of the analog eye,
     both inputs of the comparator are shifted because of this DC
     offset, and the digital eye remains unaffected.

          To achieve a robust performance and to minimize the
     sensitivity to process variation, in one embodiment, the
10   individual blocks are implemented using local feedback. Thus,
     the demodulator characteristics, such as analog eye amplitude or
     its DC level are set merely by the ratio of the resistors or
     devices which are accurately defined in an IC.

          FIG. 5 is an exemplary circuit implementation of a
15   differentiator (blocks 22 or 23 in FIG. 2), according to one
     embodiment of the present invention. The IF differentiator uses
     a single-stage operational amplifier (op-amp) followed by a
     common-source stage in a unity gain feedback, as shown in FIG.
     5. The differential inputs pairs I+, I-, Q+, and Q- are
20   connected to the differential op-amp 51 via R1, c1, R2, and C2
     respectively, where R1=R2 and C1=C2. There is a feedback loop
     from each input of the op-amp 51 to its respective output through
     transistors M1 and M2, respectively. This feedback loop
     preserves the same AC voltage at the gates of transistors M1 and
25   M3.

          Transistors M3 and M4 form the input stage of a multiplier
     (blocks 24 or 25 in FIG. 2). The values for the four transistors
     M1, M2, M3, and M4 are the same so that the same amount of
     current, I_{M3} flows through all of them. Thus, if the signal at
30   the differentiator input is V_1, the AC current flowing through
     transistors M1/M2 will be equal to:

$$i_{M1} = jC\left(w - \frac{1}{R_1 C}\right)V_i \qquad\qquad (2)$$

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1   This current is mirrored into the input devices (M3/M4) of
the multipliers which are implemented as Gilbert-type mixers,
shown in FIG. 6.

       FIG. 6 is an exemplary circuit implementation for multiplier
5   22 (I multiplier) of FIG. 2. The Q multiplier 24 has a similar
circuit implementation.   The input stage of the multiplier
(M3/M4) takes the differential input IN+ and IN- that is the
output of the BPF 21 in FIG. 2. Transistors M5/M6 and M7/M8 form
the differential pair Gilbert-type mixers that take the
10   differential input LO+ and LO- to multiply LO signal by IN
signal. As shown, the outputs of the I multiplier are connected
to the outputs of the Q multiplier (not shown) to simply form the
subtractor block 26 of FIG. 2. The common mode feedback (CMFB)
61 is used to adjust the DC output levels.

15   Assuming an ideal switching loss of 2/π and a load
resistance of R in the multipliers, the signal at the multipliers
output will be:

$$V_0 = \left(A \frac{2}{\pi} RC \right) . \phi(t) \qquad\qquad (3)$$

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       Where A is the amplitude of the signal at the differentiator
input (Vi), and φ(t) is its frequency information. In equation
2, 1/R1C is set to 2 MHz.

       Any mismatch between I and Q paths causes an incomplete
25   addition of Cos^2 and Sin^2 components at the multipliers output,
producing an undesired signal at $2\omega_{IF}$. In addition, a DC offset
at the multiplier LO or input port creates an undesired signal
at ωIF at the multiplier output. However, for 2 MHz IF, all
these spurs are located at least at 2 MHz or above, and the LPF
30   27 whose bandwidth is about 550 kHZ rejects them.

       Since the gain and center frequency of the differentiator,
as well as the bandwidth and center frequency of the filters are
determined by the RCs, an on-chip calibration circuit is designed
to adjust the RC time constants in the presence of temperature
35   and process variation, as shown in FIG. 1. In one embodiment,

1   all the capacitors are implemented as digitally-controlled binary
     array of capacitors. The RC calibration circuit tunes 1/RC to
     a reference crystal frequency.

          In this embodiment, both the post-limiter BPF and the LPF
5   after the multipliers are realized as active RC configuration.
     Therefore, their passband gain is accurately set by ratio of the
     resistors. Moreover, the input signal amplitude (A in equation
     3) is set by the limiter, which is constant over process or
     temperature variation, and is independent of the received signal
10   power. As a result, the gain of demodulator only depends on the
     differentiator gain, that is, RC, which is precisely controlled
     by the on-chip calibration circuit.

          FIG. 7 is an exemplary circuit implementation for the offset
     tracker 43 of FIG. 4. The drains of the transistors M1 & M2 is
15   connected and their sources are connected to two equal value
     resistors R. Current I1 is proportional to V_p+V_V/R, therfore
     proportional to the average of V_p and V_V. Transistors M3 and M4
     have a similar arrangement to M1 and M2 arrangement, except that
     heir gates are connected together and is driven by V_a, the analog
20   input. As a result, I2 current is proportional to $2V_a/R$.

          FIG. 8 is an exemplary simplified circuit diagram for a peak
     (or valley) detector (blocks 41 and 42 in FIG. 4). The
     peak/valley detectors take the pick (or valley) of the input
     signal as an input and charge the capacitor C to a peak (or a
25   valley) using the OpAmp 81 and the PMOS transistor M80. However,
     since the leakage current of the capacitor C is small, the
     capacitor C takes a long time to charge or discharge in response
     to changes in peaks or valleys. OpAmp 81 is a differential pair
     OpAmp with single ended output. When the signal at the input of
30   the OpAmp increases, because of the OpAmp's high gain, its output
     goes to zero which in turn, turns transistor M80 on. That pulls
     the output voltage high to adjust the peak value.

          To ameliorate the slow nature of the peak/valley detectors,
     two time constants, namely fast attack and slow decay, are
35   assigned to the detectors, as shown in FIG. 8. At the receiver

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1   start-up, the detectors are switched to fast attack mode by fast
     switch S1 that is connected to a large current sink, regulating
     their outputs quickly to the peak and valley of the received
     analog eye. Once this initial adjustment is accomplished, the
5   detectors switch to slow decay mode by S2 that is connected to
     a small current sink, where the peak/valley detector capacitor
     C at the OUT node is slowly discharged by the leakage current I
     $_{small}$. These time constants are adaptively set by detecting the
     received eye amplitude, and based on the receiver start-up signal
10   through controlling the timing of the two switches S1 and S2.

          In one embodiment, an FSK demodulator for use in various
     applications including Bluetooth is implemented in a 0.35 μm
     CMOS process. The entire exemplary demodulator, integrated as
     a part of a low-IF receiver with 2 MHz intermediate frequency,
15   consumes 3 mA from 2.7 V supply. The required signal-to-noise
     ratio (SNR) for 0.1 % bit error rate (BER) is about 18 dB in this
     implementation.

          It will be recognized by those skilled in the art that
     various modifications may be made to the illustrated and other
20   embodiments of the invention described above, without departing
     from the broad inventive scope thereof. It will be understood
     therefore that the invention is not limited to the particular
     embodiments or arrangements disclosed, but is rather intended to
     cover any changes, adaptations or modifications which are within
25   the scope of the invention as defined in the claims.

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